

## CLAIMS

*What is claimed is:*

- 1 1. A reference cell for determining a state stored in a first memory cell, comprising:  
2 a second memory cell that produces a current; and  
3 a current reduction element that  
4 is coupled to the memory cell,  
5 is configured to receive a reference voltage, and  
6 has a resistance that varies as a function of the reference voltage.
- 1 2. The reference cell of claim 1, wherein the second memory cell is a TCCT based memory cell.
- 1 3. The reference cell of claim 1, wherein the second memory cell is an SRAM memory cell.
- 1 4. The reference cell of claim 1, wherein the second memory cell is an MRAM memory cell.
- 1 5. The reference cell of claim 1, wherein the second memory cell is a memory cell with a  
2 floating gate.
- 1 6. The reference cell of claim 1, wherein the current reduction element is a transistor.

1

- 1 7. A reference cell for a TCCT based memory cell, comprising:  
2 an NDR device including  
3 a first end configured to have a first voltage applied thereto,  
4 a second end,  
5 a doped semiconductor layer between the first and second ends, and  
6 a gate-like device disposed adjacent to the doped semiconductor layer;  
7 a first word line;  
8 a second word line coupled to the gate-like device;  
9 a pass transistor including  
10 a drain,  
11 a source coupled to the second end, and  
12 a gate coupled to the first word line;  
13 a bit line; and  
14 a current reduction element coupled between the bit line and the drain.
- 1 8. The reference cell of claim 7 wherein the current reduction element is a second pass transistor  
2 including a gate having a second voltage applied thereto.

- 1 9. A circuit to generate a reference voltage, comprising:  
2 a memory cell configured to generate a first current;  
3 a reference cell configured to generate a second current; and  
4 a feedback circuit configured to  
5 compare the first current to the second current, and  
6 generate a reference voltage in response thereto.
- 1 10. The circuit of claim 9 wherein the reference cell is configured to receive the reference  
2 voltage.
- 1 11. The circuit of claim 10 wherein the second current varies as a function of the reference  
2 voltage.
- 1 12. The circuit of claim 11 wherein the reference cell includes a pass transistor configured to  
2 receive the reference voltage.
- 1 13. The circuit of claim 12 wherein the memory cell includes a pass transistor having a first W/L  
2 ratio.
- 1 14. The circuit of claim 13 wherein the pass transistor of the reference cell has a second W/L  
2 ratio equal to about twice the first W/L ratio.

- 1 15. A circuit to generate a reference voltage, comprising:  
2 a memory cell configured to generate a first current;  
3 a first reference cell configured to generate a second current;  
4 a second reference cell configured to generate a third current; and  
5 a feedback circuit configured to  
6 compare the first current to the sum of the second and third currents, and  
7 generate a reference voltage in response thereto.
- 1 16. The circuit of claim 15 wherein the first and second reference cells are each configured to  
2 receive the reference voltage.
- 1 17. The circuit of claim 16 wherein the second and third currents vary as a function of the  
2 reference voltage.
- 1 18. The circuit of claim 15 wherein the memory cell is a TCCT based memory cell and includes  
2 an NDR device coupled to a first pass transistor.
- 1 19. The circuit of claim 15 wherein multiple memory cells generate the first current, multiple  
2 first reference cells generate the second current, and multiple second reference cells  
3 generate the third current.

- 1    20. The circuit of claim 15 wherein the first and second reference cells each include  
2                    an NDR device,  
3                    a first pass transistor coupled to the NDR device, and  
4                    a second pass transistor coupled to the first pass transistor.
- 1    21. The circuit of claim 20 wherein each second pass transistor has a gate configured to receive  
2                    the reference voltage.
- 1    22. The circuit of claim 21 wherein the feedback circuit maintains the sum of the second and  
2                    third currents equal to the first current by adjusting the reference voltage.
- 1    23. The circuit of claim 15 wherein the feedback circuit includes a current comparator coupled  
2                    to a ramp output voltage generator.
- 1    24. The circuit of claim 15 wherein the memory cell is an SRAM cell that includes a pass  
2                    transistor.
- 1    25. The circuit of claim 15 wherein the memory cell is a floating gate based memory cell that  
2                    includes a pass transistor.
- 1    26. The circuit of claim 15 wherein the memory cell is an MRAM cell that includes a pass  
2                    transistor.

1 27. A circuit to generate a reference voltage to control a current output of a reference cell,  
2 comprising:  
3 a TCCT based memory cell including an NDR device and configured to generate a first  
4 current;  
5 a first reference cell configured to generate a second current and including  
6 an NDR device, and  
7 a pass transistor coupled to the NDR device;  
8 a second reference cell configured to generate a third current and including  
9 an NDR device, and  
10 a pass transistor coupled to the NDR device; and  
11 a feedback circuit configured to  
12 compare the first current to the sum of the second and third currents, and  
13 generate a reference voltage in response thereto.

1 28. The circuit of claim 27 wherein the pass transistors of the first and second reference cells  
2 each have a gate configured to receive the reference voltage.

1 29. The circuit of claim 28 wherein the feedback circuit maintains the sum of the second and  
2 third currents equal to the first current by adjusting the reference voltage.

1 30. The circuit of claim 29 wherein the feedback circuit maintains the sum of the currents from  
2 more than two memory elements equal to the first current by adjusting the reference  
3 voltage.

1 31. The circuit of claim 27 wherein the feedback circuit includes a current comparator coupled  
2 to a ramp output voltage generator.

1 32. A memory array comprising:  
2 a memory cell having a state and configured to generate a first current on a first bit line;  
3 a circuit configured to generate a reference voltage;  
4 a reference cell configured to receive the reference voltage and to generate a second  
5 current on a second bit line; and  
6 means for determining the state of the memory cell by comparing the first current to the  
7 second current.

1 33. The memory array of claim 32 wherein the memory array further comprises first and second  
2 word lines and the memory cell is a TCCT based memory cell including  
3 a first NDR device disposed adjacent to the second word line, and  
4 a first pass transistor with a gate coupled to the first word line.

1 34. The memory array of claim 32 wherein the reference cell includes  
2 an NDR device disposed adjacent to the second word line, and  
3 a pass transistor having a gate with the reference voltage applied thereto.

1 35. The memory array of claim 32 wherein the means for determining a state of the TCCT based  
2 memory cell is a sense amplifier.

1 36. The memory array of claim 32 wherein the memory cell is an SRAM memory cell and the  
2 means for determining a state of the SRAM cell is a sense amplifier.

1 37. The memory array of claim 32 wherein the memory cell is an MRAM memory cell and the  
2 means for determining a state of the MRAM cell is a sense amplifier.

1 38. The memory array of claim 32 wherein the memory cell is a memory cell with a floating  
2 gate and the means for determining a state of the memory cell with a floating gate is a  
3 sense amplifier.



1 39. A memory array comprising:

2 a first bit line;

3 a second bit line;

4 a first word line;

5 a second word line;

6 a TCCT based memory cell including

7 a first NDR device disposed adjacent to the second word line and having

8 a first end having a first voltage applied thereto, and

9 a second end;

10 a first pass transistor having

11 a source coupled to the second end of the first NDR device,

12 a drain coupled to the first bit line, and

13 a gate coupled to the first word line; and

14 a reference cell including

15 a second NDR device disposed adjacent to the second word line and having

16 a first end having the first voltage applied thereto, and

17 a second end;

18 a second pass transistor having

19 a source coupled to the second end of the second NDR device,

20 a drain, and

21 a gate coupled to the first word line;

22 a current reduction element coupled between the second bit line and the drain of

23 the second pass transistor; and

24 means for determining a state of the TCCT based memory cell by comparing a first

25 current on the first bit line and a second current on the second bit line.

1 40. The memory array of claim 39 wherein the means for determining a state of the TCCT based

2 memory cell is a sense amplifier.

1 41. The memory array of claim 39 further including a circuit to generate a reference voltage to  
2 control the second current.

1 42. The memory array of claim 41 wherein the reference voltage is applied to the current  
2 reduction element.

1 43. The memory array of claim 42 wherein the current reduction element is a third pass  
2 transistor.

1 44. A memory device, comprising:

2 at least one memory array including

3 at least one TCCT based memory cell;

4 at least one reference cell; and

5 a sense amplifier configured to

6 receive a memory cell current produced by the at least one TCCT based  
7 memory cell,

8 receive a reference cell current produced by the at least one reference cell,

9 and

10 compare the memory cell current with the reference cell current to

11 determine a state of the at least one TCCT based memory cell.

1 45. A method for producing a reference current, comprising:  
2 providing a reference cell including  
3 an NDR device configured to produce a current, and  
4 a pass transistor connected to the NDR device and having a gate;  
5 providing a circuit configured to produce a reference voltage; and  
6 applying the reference voltage to the gate.

1 46. The method of claim 45 wherein providing a circuit includes  
2 providing a memory cell producing a first current;  
3 providing a first circuit reference cell producing a second current;  
4 providing a second circuit reference cell producing a third current; and  
5 comparing the first current with the sum of the second and third currents.

1 47. The method of claim 46 wherein providing a circuit further includes applying the reference  
2 voltage to the first and second circuit reference cells.

1 48. The method of claim 47 wherein providing a circuit further includes adjusting the reference  
2 voltage to maintain the sum of the second and third currents equal to the first current.

1

1 49. A method for producing a reference current for determining a state of a TCCT based  
2 memory cell, comprising:  
3 generating a first current by a first TCCT based memory cell; and  
4 adjusting the first current to produce the reference current.

1 50. The method of claim 49 wherein adjusting the first current includes generating a reference  
2 voltage.

1 51. The method of claim 50 wherein generating the reference voltage includes  
2 generating a second current by a second TCCT based memory cell,  
3 generating a third current by a third TCCT based memory cell, and  
4 comparing the second current to the third current.

1 52. The method of claim 51 wherein the third current varies a function of the reference voltage.

1 53. The method of claim 52 wherein comparing the second current to the third current includes  
2 determining whether the third current is about half of the second current.

1 54. The method of claim 53 wherein determining whether the third current is about half of the  
2 second current includes  
3 generating a fourth current by a fourth TCCT based memory cell wherein the fourth  
4 current varies a function of the reference voltage and is substantially the same as  
5 the third current, and  
6 comparing the sum of the third and fourth currents to the second current.

1 55. A method for reading a state of a memory cell, comprising:  
2 operating the memory cell to produce a first current on a first bit line;  
3 operating a reference cell to produce a second current on a second bit line;  
4 operating a circuit to provide a reference voltage to the reference cell; and  
5 comparing the first and second currents to determine the state of the memory cell.

1 56. The method of claim 55 wherein the memory cell is a TCCT based memory cell and  
2 operating the memory cell includes applying a first voltage to one end of the TCCT based  
3 memory cell.

1 57. The method of claim 56 wherein operating the memory cell further includes applying a  
2 second voltage to a gate of a pass transistor of the TCCT based memory cell.

1 58. The method of claim 55 wherein operating the reference cell includes applying a first  
2 voltage to one end of the reference cell.

1 59. The method of claim 58 wherein operating the reference cell further includes applying a  
2 second voltage to a gate of a pass transistor of the reference cell.

1 60. The method of claim 59 wherein the second voltage is the reference voltage.

1 61. The method of claim 55 wherein operating the circuit includes  
2 operating a circuit memory cell configured to produce a third current;  
3 operating a circuit reference cell configured to produce a fourth current; and  
4 using a feedback circuit configured to  
5 receive the third and fourth currents,  
6 provide the reference voltage to the circuit reference cell, and  
7 adjust the reference voltage such that the fourth current is about half of the third  
8 current.